REMARKS

Applicants respectfully request reconsideration of the present application in view of this response. Claims 1-18 are currently pending. Of those, claims 1-13 and 15-18 have been amended and claims 1, 11, 17 and 18 are independent claims.

PRIORITY DOCUMENTS

Applicants appreciate the Examiner's acknowledgement of Applicants' claim for priority under 35 U.S.C. § 119, and the indication that all necessary priority documents have been received.

DRAWINGS

Applicants appreciate the Examiner's acceptance of the drawings filed on December 23, 2003.

INFORMATION DISCLOSURE STATEMENT

Applicants appreciate and acknowledge the Examiners careful consideration of the references cited in the Information Disclosure Statement filed December 23, 2003, as indicated by the Examiner's initials and signature on the form PTO-1449.

CLAIM AMENDMENTS

As noted above, Applicants have amended claims 1-13 and 15-18 by way of this response. However, Applicants respectfully submit that all such amendments made to claims 1-13 and 15-18 are non-narrowing, have not been made to overcome any prior art rejection and have been made for no other reason than to put claims 1-18 more in accordance with current United States Patent and Trademark Office Practice.

PRIOR ART REJECTIONS

Rejections under 35 U.S.C. §103(a)

Claims 1, 2, 11-13, 17 and 18 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Shimada (U.S. Patent No. 6,219,017) in view of Nakanishi (U.S. Patent No. 5,488,389). Applicants respectfully traverse this rejection.

Lack of Motivation to Combine Reference Teachings

Initially, the Examiner has not supplied the requisite evidence to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a).

On page 2 of the Office Action, the Examiner correctly recognizes that Shimada fails to teach at least, "interpolating video signals for the previous field before modulating the driving signals, so as to generate video signals of one frame," and "interpolating video signals for the current field before modulating the driving signals, so as to generate video signals of one frame," as set forth in claim 1, but alleges it would have been obvious to the skilled

artisan to "utilize the multiple memory and line doubling, taught by Nakanishi, in the display modulation controls taught by Shimada." See page 3 of the Office Action. In so doing, the Examiner alleges that the combination of Shimada and Nakanishi would "allow for the deinterlacing of the input video signal with greater speed... for the benefit of faster deinterlacing." See page 3 of the Office Action. Applicants respectfully disagree.

The Examiner's reasoning amounts to nothing more than a classic "could have" combined argument: The test for obviousness, however, is "would have." The mere fact that Shimada and Nakanishi may arguably be from the same field of endeavor and the "multiple memory and line doubling, taught by Nakanishi," could arguably improve deinterlacing speed of an input video signal, is not sufficient to establish why the skilled artisan would look to Nakanishi for the deficiencies of Shimada with respect to claim 1, for example.

From the Examiner's above reasoning, any combination of references under 35 U.S.C. § 103(a), which could, potentially, produce an arguable advantage would be proper. However, as the Examiner is aware, this is clearly not the case. In combining references under 35 U.S.C. § 103(a), the Examiner must supply evidence of the necessary motivation needed to lead one of ordinary skill in the art to combine the teachings of Shimada and Nakanishi as forth in two cases decided by the Court of Appeals for the Federal Circuit (CAFC), In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed.Cir. 1999) and In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed.Cir. 2000). However, Applicants submit that the Examiner has clearly failed to do

so and, as such, a *prima facie* case of obviousness has not been properly established.

In addition, Shimada is directed to reducing manufacturing costs of LCD display apparatuses, for example, by reducing components included therein. See col. 4, ll. 66 – col. 5, ll. 2 of Shimada. Furthermore, in order to accomplish that which the Examiner contends (i.e., incorporating the interpolation of Nakanishi into the system of Shimada), additional components, for example, an additional field memory for line doubling must be added. However, Applicants respectfully submit that adding any additional components to the system of Shimada would increase the cost of manufacturing the LCD display of Shimada and, thereby, destroy at least one of the intended purposes of Shimada.

Furthermore, carrying out modulation before interpolation (e.g., as claimed in claim 1) is easier in terms of circuitry, since the circuit scale is reduced. If the interpolation (e.g., IP transformation) is carried out first, the necessary amount of memory (e.g., for storing a previous field) is doubled, because the interpolation doubles the amount of data.

When data corresponding to one line of the current field is continuously output twice (another interpolating method), only a memory corresponding to at least one line is necessary. As such, Applicants submit that without using the present application as a blueprint for piecing together the prior art to defeat patentability, it would not be have been obvious for one skilled in the art to arrive at simplified circuitry by performing modulation before interpolation. Using the present application as a blueprint for piecing together the prior art is

the essence of improper hindsight reconstruction. Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed.Cir. 1999).

Moreover, Nakanishi discloses de-interlacing a video signal, for example, by repeating the lines of a field to "fill" the "unused" lines in that field.

As a simplified example:

Input

Field 1	Field 2
L1	
	L2
L3	
	L4
L5	

→

Output

Field 1	Field 2
L1	
L1	L2
L3	L2
L3	L4
L5	L4

Shimada discloses a device for displaying high resolution images using a wobbling apparatus, whereby the output from the pixels is shifted by a small amount in odd fields to effectively increase the resolution. See Figures 2A and 2B of Shimada, for example. In this case, the LCD pixels in an odd field (dashed lines in Figure 2B of Shimada) and the LCD pixels in an even field (solid lines in Figure 2B of Shimada) are the same pixels (see Figure 6 of Shimada, for example). Therefore, the "solid" and "dashed" pixels of Figure 2B cannot be displayed at the same time.

As a result, the fields of Shimada and Nakanishi cannot be equivalent, since the filling of the field, according to Nakanishi, is undesirable in the device of Shimada, because the filled pixels cannot be displayed in the same field.

Therefore, given that the fields of Shimada are not equivalent to the fields of Nakanishi, it is clear that the devices of Shimada and Nakanishi cannot be combined so as to operate according to their intended purposes. For example, Shimada is directed to mitigating the degradation in image quality due to delay response in an LCD and TN cell (See Abstract). However, since the fields of Shimada and Nakanishi are not equivalent, at least four fields are required. This would reduce the time allowed for the LCD and TN cells to respond by half, and subsequently degrade display quality.

Simply put, combining the devices of Nakanishi and Shimada is impossible, without some inventive contribution to make the devices compatible. Therefore, the ordinary skilled person would not apply the teachings of Nakanishi to those of Shimada.

In view of the above, Applicants submit that the skilled artisan would not look to Nakanishi for the deficiencies of Shimada with regard to claim 1.

Features of Claim 1 Lacking

On page 2 of the Office Action, the Examiner relies upon FIG. 13 and col. 3, ll. 59-63 of Shimada to allegedly teach "generating driving signals based on video signals of a current field," and modulating the driving signals "by referring to video signals of a previous field," as set forth in claim 1. However, Applicants respectfully disagree.

As shown in FIG. 13 of Shimada, a correction circuit 7 receives a current video signal I_n and a previous video signal I_{n-1}, the previous video signal I_{n-1}

being output from a memory 8. Upon reception, the correction circuit 7 outputs correction signals V_n, H_n considering both the current video signal I_n and the previous video signal I_{n-1}. The correction signal H_n is then output to an LCD 13.

However, the system of Shimada, as illustrated in FIG. 13, does not generate "driving signals based on video signals of a current field," and modulate the driving signals "by referring to video signals of a previous field," as set forth in claim 1. Shimada makes no mention or suggestion of any modulating of driving signals "by referring to video signals of a previous field," as set forth in claim 1. Instead, Shimada merely teaches that the correction circuit 7 outputs correction signals H_n considering the current video signal I_n and the previous video signal I_{n-1}. Thus, at most, Shimada teaches generating correction signals based on current video signal I_n and the previous video signal I_{n-1}.

Furthermore, as noted above, on page 2 of the Office Action, the Examiner correctly recognizes that Shimada fails to teach or suggest at least, "interpolating video signals for the previous field before modulating the driving signals, so as to generate video signals of one frame," and "interpolating video signals for the current field before modulating the driving signals, so as to generate video signals of one frame," as set forth in claim 1, and relies upon Nakanishi to allegedly teach these features. However, even assuming *arguendo* that Shimada could be combined with Nakanishi (which Applicants do not admit for at least the reasons set forth above), there is no teaching in any of the

references that the interpolating step should be carried out before the modulating step.

The Examiner asserts that this is taught by Nakanishi, but does not clearly indicate the supposed basis for this teaching. Furthermore, the modulation is not present in Nakanishi, and as such, Nakanishi cannot teach that interpolating should be carried out before the modulation, as in claim 1, for example. Similarly, Shimada cannot make up for this deficiency, since interpolation is not taught by Shimada.

Accordingly, Applicants respectfully submit that neither Shimada nor Nakanishi, neither alone nor in combination, teaches or suggests all of the features set forth in claim 1.

Applicants respectfully submit that claims 11, 17 and 18 are also allowable for at least reasons somewhat similar to those set forth above with regard to claim 1. However, these claims should be interpreted solely by the limitations presented therein.

With regard to claims 2, 12 and 13, Applicants submit that these claims are allowable at least by virtue of their dependency on claim 1 or 11.

Rejection under 35 U.S.C. § 103(a)

Claims 3-5 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Shimada (U.S. Patent No. 6,219,017) in view of Nakanishi (U.S. Patent No. 5,488,389) and further in view of Huang (U.S. Patent No. 6,295,091). Applicants respectfully traverse this rejection.

On page 7 of the Office Action, the Examiner correctly recognizes that neither Shimada nor Nakanishi teach nor suggest video signals, which are "interpolated for a respective line of a field other than a target field of interpolation in such a manner that the interpolated video signals contain the same information as video signals obtained by averaging target field video signals respectively of a pair of frame lines adjacent to the interpolated line," as set forth in claim 3, and somewhat similarly in claims 4 and 5. The Examiner relies upon Huang to allegedly teach these features. However, even assuming *arguendo* that Huang could be combined with Shimada and Nakanishi (which Applicants do not admit for at least reasons somewhat similar to those set forth above with regard to Shimada and Nakanishi), Applicants respectfully submit that Huang still fails to at least make up for the deficiencies of Shimada and Nakanishi with respect to claim 1.

Accordingly, Applicants submit that claims 3-5 are in condition for allowance.

Rejection under 35 U.S.C. § 103(a)

Claims 6-8, 15 and 16 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Shimada (U.S. Patent No. 6,219,017) in view of Nakanishi (U.S. Patent No. 5,488,389) and further in view of Mizumaki (U.S. Patent No. 6,333,727). Applicants respectfully traverse this rejection.

On page 10 of the Office Action, the Examiner correctly recognizes that neither Shimada nor Nakanishi teach nor suggest at least "adjusting strength

of modulation in said modulating step by referring to a result of comparison between video signals of the current field and video signals of an earlier of previous two fields," as set forth in claim 6 and somewhat similarly in claims 15 and 16. The Examiner relies upon Mizumaki to allegedly teach these features. However, even assuming *arguendo* that Mizumaki could be combined with Shimada and Nakanishi (which Applicants do not admit for at least reasons somewhat similar to those set forth above with regard to Shimada and Nakanishi), Applicants respectfully submit that Mizumaki would still fail to at least make up for the deficiencies of Shimada and Nakanishi with respect to claim 1.

Accordingly, Applicants submit that claims 6, 15 and 16 are in condition for allowance. Applicants submit that claims 7 and 8 are in condition for allowance at least by virtue of there dependency on claim 6.

Rejection under 35 U.S.C. § 103(a)

Claims 9 and 10 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Shimada (U.S. Patent No. 6,219,017) in view of Nakanishi (U.S. Patent No. 5,488,389) and further in view of Gadeyne et al. (U.S. Patent No. 6,909,472, hereinafter referred to as "Gadeyne"). Applicants respectfully traverse this rejection.

On page 17 of the Office Action, the Examiner correctly recognizes that neither Shimada nor Nakanishi teach nor suggest at least features set forth in claim 9. The Examiner relies upon Gadeyne to allegedly teach these features.

However, even assuming *arguendo* that Gadeyne could be combined with Shimada and Nakanishi (which Applicants do not admit for at least reasons somewhat similar to those set forth above with regard to Shimada and Nakanishi), Applicants respectfully submit that Gadeyne would still fail to at least make up for the deficiencies of Shimada and Nakanishi, as discussed above, with respect to claim 1.

Accordingly, Applicants submit that claim 9 is in condition for allowance. Further, Applicants submit that claim 10 is in condition for allowance at least by virtue of its dependency on claim 9.

Rejection under 35 U.S.C. § 103(a)

Claim 14 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Shimada (U.S. Patent No. 6,219,017) in view of Nakanishi (U.S. Patent No. 5,488,389) and further in view of Choquet et al. (U.S. Patent No. 4,937,667, hereinafter referred to as "Choquet"). Applicants respectfully traverse this rejection.

On page 19 of the Office Action, the Examiner correctly recognizes that neither Shimada nor Nakanishi teach nor suggest features as set forth in claim 14. The Examiner relies upon Choquet to allegedly teach these features. However, even assuming *arguendo* that Choquet could be combined with Shimada and Nakanishi (which Applicants do not admit for at least reasons somewhat similar to those set forth above with regard to Shimada and Nakanishi), Applicants respectfully submit that Choquet would still fail to at

least make up for the deficiencies of Shimada and Nakanishi, as discussed above, with respect to claim 1.

Accordingly, Applicants submit that claim 14 is in condition for allowance.

CONCLUSION

In view of above remarks, reconsideration of the outstanding rejection and allowance of the pending claims is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Andrew M. Waxman, Reg. No. 56,007, at the number of the undersigned listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, PLC

By _____
Donald J. Daley
Reg. No. 34,313

DJD/HRH/AMW:jcp

P.O. Box 8910
Reston, VA 20195
(703) 668-8000